What is claimed is:

1. An apparatus for processing bytes received from a data stream, comprising:

a plurality of parallel byte processing engines for receiving a first plurality of bytes from a data channel during a first cycle and for generating byte status data for each of said first plurality of bytes; and

an input formatter, coupled to said plurality of parallel byte processing engines, for receiving said byte status data from said plurality of parallel byte processing engines, wherein if one of said byte status data received from one of said plurality of byte processing engines indicates a flag byte, at least one of said first plurality of bytes processed by a neighboring byte processing engine is designated as a delineation byte.

2. The apparatus of claim 1 further comprising a plurality of byte status registers, each coupled to a respective one of said plurality of byte processing engines, each storing byte status data for a respective one of a prior plurality of bytes received by said plurality of parallel byte processing engines from said data channel during a prior cycle, wherein said input formatter designates a last byte of said prior plurality of bytes as an end delineation byte if said last byte is not a flag byte and a first byte of said first plurality of bytes is a flag byte.

3. The apparatus of claim 1 further comprising a plurality of byte status registers, each coupled to a respective one of said plurality of byte processing engines, each storing byte status data for a respective one of a prior plurality of bytes received by said plurality of parallel byte processing engines from said data channel during a prior cycle, wherein said input formatter designates a first byte of said first plurality of bytes as a start delineation byte if said first byte is not a flag byte and a last byte of said prior plurality of bytes is a flag byte.

4. The apparatus of claim 1 wherein said byte status data includes a write enable status bit for respective ones of said first plurality of bytes identified as valid data, and wherein said input formatter further generates a byte status code for each of said first plurality of bytes identified as valid data, wherein said byte status code identifies at least one of said first plurality of bytes as a delineation byte.

5. The apparatus of claim 4 further comprising an input register FIFO, coupled to said input formatter, for storing said first plurality of bytes identified as valid data and corresponding byte status codes for each of said stored bytes.

6. The apparatus of claim 1 further comprising:

a plurality of data registers, each coupled to a respective one of said plurality of parallel byte processing engines, each for storing a byte value of a respective one of a prior plurality of bytes received by said plurality of parallel byte processing engines from said data channel during a prior cycle;

a plurality of parallel quad-byte processors, each coupled to at least one of said plurality of data registers, for calculating respective cell delineation values; and

a plurality of comparators, each coupled to a respective one of said plurality of parallel quad-byte processors and a respective one of said plurality of parallel byte processing engines, wherein each of said plurality of comparators receives a respective one of said first plurality of bytes from a respective one of said parallel byte processing engines and compares a respective one of said first plurality of bytes to a respective one of said cell delineation values to determine whether a respective one of said prior plurality of bytes constitutes an ATM start byte.

7. An apparatus for processing bytes received from a data stream, comprising:

parallel byte processing means for receiving a first plurality of bytes from a data channel during a first cycle and for generating byte status data for each of said first plurality of bytes; and

an input formatter means, coupled to said parallel byte processing means, for receiving said byte status data from said parallel byte processing means, wherein if a

respective one of said first plurality of bytes is identified as a flag byte, a neighboring one of said first plurality of bytes is designated as a delineation byte.

8. The apparatus of claim 7 further comprising a status register means, coupled to said parallel byte processing means, for storing byte status data for a prior plurality of bytes received by said parallel byte processing means from said data channel during a prior cycle, wherein said input formatter means designates a last byte of said prior plurality of bytes as an end delineation byte if said last byte is not a flag byte and a first byte of said first plurality of bytes is a flag byte.

9. The apparatus of claim 7 further comprising a status register means, coupled to said parallel byte processing means, for storing byte status data for a prior plurality of bytes received by said parallel byte processing means from said data channel during a prior cycle, wherein said input formatter means designates a first byte of said first plurality of bytes as a start delineation byte if said first byte is not a flag byte and a last byte of said prior plurality of bytes is a flag byte.

10. The apparatus of claim 7 wherein said byte status data includes a write enable status bit for respective ones of said first plurality of bytes identified as valid data, and wherein said input formatter means further generates a byte status code for each of said first plurality of bytes identified as valid data, wherein said byte status code identifies at least one of said first plurality of bytes as a delineation byte.

11. The apparatus of claim 10 further comprising an input register means, coupled to said input formatter means, for storing said first plurality of bytes identified as valid data and corresponding byte status codes for each of said stored bytes.

12. The apparatus of claim 7 further comprising:

data register means, coupled to said parallel byte processing means, for storing byte values for a prior plurality of bytes received by said parallel byte processing means from said data channel during a prior cycle;

parallel quad-byte processing means, coupled to said data register means, for calculating respective cell delineation values; and

comparator means, coupled to said parallel quad-byte processing means and to said parallel byte processing means, for receiving said first plurality of bytes from said parallel byte processing means and comparing a respective one of said first plurality of bytes to a respective one of said cell delineation values to determine whether a respective one of said prior plurality of bytes constitutes an ATM start byte.

13. A method of processing bytes received from a data stream, comprising:

receiving a first plurality of bytes from a data channel during a first cycle;

generating byte status data for each of said first plurality of bytes, wherein said byte status data indicates whether one of said first plurality of bytes constitutes a flag byte; and

processing said byte status data, wherein if a respective one of said first plurality of bytes is identified as a flag byte, a neighboring one of said first plurality of bytes is designated as a delineation byte.

14. The method of claim 13 further comprising:

storing byte status data for a respective one of a prior plurality of bytes, received from said data channel during a prior cycle, in a first buffer; and

designating a last byte of said prior plurality of bytes as an end delineation byte if said last byte is not a flag byte and a first byte of said first plurality of bytes is a flag byte.

15. The method of claim 13 further comprising:

storing byte status data for a respective one of a prior plurality of bytes, received from said data channel during a prior cycle, in a first buffer; and

designating a first byte of said first plurality of bytes as a start delineation byte if said first byte is not a flag byte and a last byte of said prior plurality of bytes is a flag

byte.

16. The method of claim 13 wherein said byte status data includes a write enable status bit for respective ones of said first plurality of bytes identified as valid data, and wherein said method further comprises generating a byte status code for each of said first plurality of bytes identified as valid data, wherein said byte status code identifies at least one of said first plurality of bytes as a delineation byte.

17. The method of claim 16 further comprising storing said first plurality of bytes identified as valid data and corresponding byte status codes for each of said stored bytes in a second buffer.

18. The method of claim 13 further comprising:

storing byte values for a prior plurality of bytes, received from said data channel during a prior cycle, in a data buffer;

calculating respective cell delineation values using at least one of said stored byte values for each calculation; and

comparing a respective one of said first plurality of bytes to a respective one of said cell delineation values to determine whether a respective one of said prior plurality of bytes constitutes an ATM start byte.